High Voltage Output Hysteretic Mode Step Up DC/DC Controller

Features

- Wide output voltage range: 6V to 500V
- Low input voltage: 2.7V
- 5W maximum output power with external MOSFET driver
- Built-in charge pump converter for the gate driver
- Programmable switching frequency from 40kHz to 400kHz
- Four programmable duty cycles from 50% to 87.5%
- FB return ground switch for power savings applications
- Built-in delay timer for internal protection
- Non-isolated DC/DC converter
- Processed with HVCMOS® technology

Applications

- Portable electronic equipment
- MEMS
- Printers

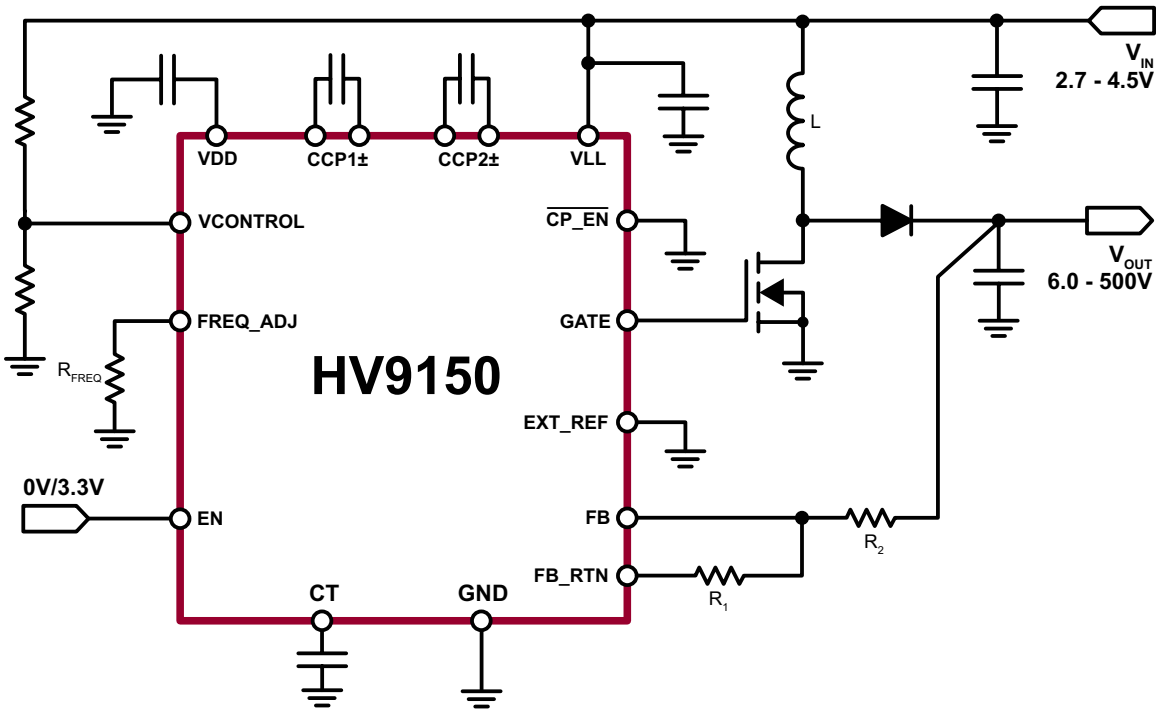
General Description

The HV9150 is a high output voltage hysteretic mode step up DC/DC controller that has both a built-in charge pump converter and a linear regulator for a wide range of input voltage. The charge pump converter mode is ideal for battery powered applications. The internal converter can provide a minimum of 5.0V gate driver output voltage (at V_{IN} = 2.7V) to the external N-channel MOSFET. The range of 2.7V to 4.5V input supply voltage is ideal for battery powered applications such as portable electronics equipment. The internal linear regulator is selected when a higher supply voltage rail is available in the system.

A feedback return ground path switch is also integrated in the device to minimize the quiescent current during the controller shutdown. This feature provides power savings for energy critical applications.

In addition, a built-in timer is available to protect the internal circuit and to help dissipate the energy from the external high voltage storage capacitor. This device is designed for systems requiring high voltage and low current applications such as MEMS devices.

Block Diagram



Ordering Information

Part Number	Package Option	Packing
HV9150K6-G	16-Lead (3x3) QFN	3000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

Absolute Maximum Ratings*

Parameter	Value
V_{LL}, Input voltage supply	-0.5V to 5.0V
V_{DD}, Charge pump output voltage	-0.5V to 13.6V
Logic input levels	-0.5V to V_{LL} +0.5V
Continuous power dissipation *(Note: on a 3" by 4" FR4 PCB @T_a = 25°C)*	3000mW
Junction temperature range	-25°C to +125°C
Storage temperature range	-65°C to +125°C

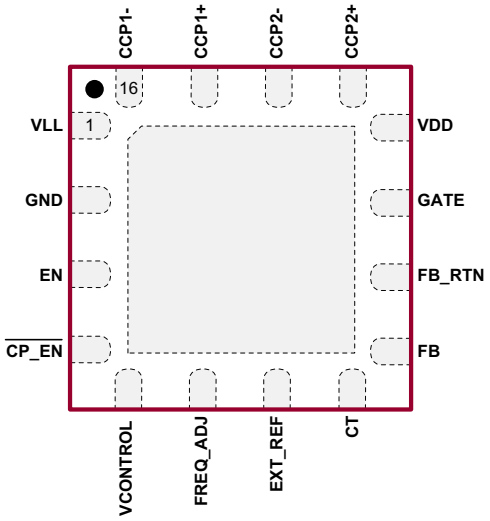
** All voltages referenced to device GND.*

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Typical Thermal Resistance

Package	θ_{ja}
16-Lead QFN	33°C/W

Pin Configuration



16-Lead QFN
(top view)

Note: *Pads are at the bottom of the package. Center heat slug is at ground potential.*

Product Marking

Y = Last Digit of Year Sealed
W = Code for Week Sealed
L = Lot Number
____ = "Green" Packaging

Package may or may not include the following marks: Si or 

16-Lead QFN

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{LL}	Input voltage (CP mode)	2.7	-	4.5	V	---
V_{IH}	High-level input voltage	0.8V_{LL}	-	V_{LL}	V	---
V_{IL}	Low-level input voltage	0	-	0.2V_{LL}	V	---

Power-Up and Power-Down Sequence

Power-up sequence should be the following:

1. Connect ground.
2. Apply V_{IN}.
3. Set all inputs to a known state.

Power-down sequence should be the reverse of the above.

DC Electrical Characteristics

(Over recommended operating supply voltages and temperatures unless otherwise noted, T_J = 25°C)

Sym	Description		Min	Typ	Max	Unit	Conditions
Power Supply							
$I_{LLQ(off)}$	Quiescent V_{LL} supply current (EN = ”0”)		-	-	2.0	µA	---
$I_{LL(on)}$	V_{LL} supply current (EN = ”1”)	GATE = NC	-	-	1.5	mA	f_{OSC} = 100kHz, V_{LL} = 4.5V
		GATE = 300pF	-	-	4.0		
$I_{DD(on)}$	V_{DD} supply current (EN = ”1”)	GATE = NC	-	-	1.0	mA	f_{OSC} = 100kHz, V_{DD} = 12.6V
		GATE = 300pF	-	-	2.5		
$I_{DDQ(off)}$	Quiescent V_{DD} supply current (EN = ”0”)		-	-	2.0	µA	---
I_{IH}	High-level logic input current		-	-	1.0	µA	V_{IH} = V_{LL}
I_{IL}	Low-level logic input current		-	-	-1.0	µA	V_{IL} = 0V
GATE	GATE driver output voltage	V_{LL} = 4.5V GATE = NC	10.2	-	12.3	V	---
		V_{LL} = 2.7V GATE = NC	5.0	-	6.9		
$V_{LL(LDO)}$	Linear regulator output voltage		3.0	-	3.6	V	---

AC Electrical Characteristics

(Over recommended operating supply voltages and temperatures unless otherwise noted, T_J = 25°C)

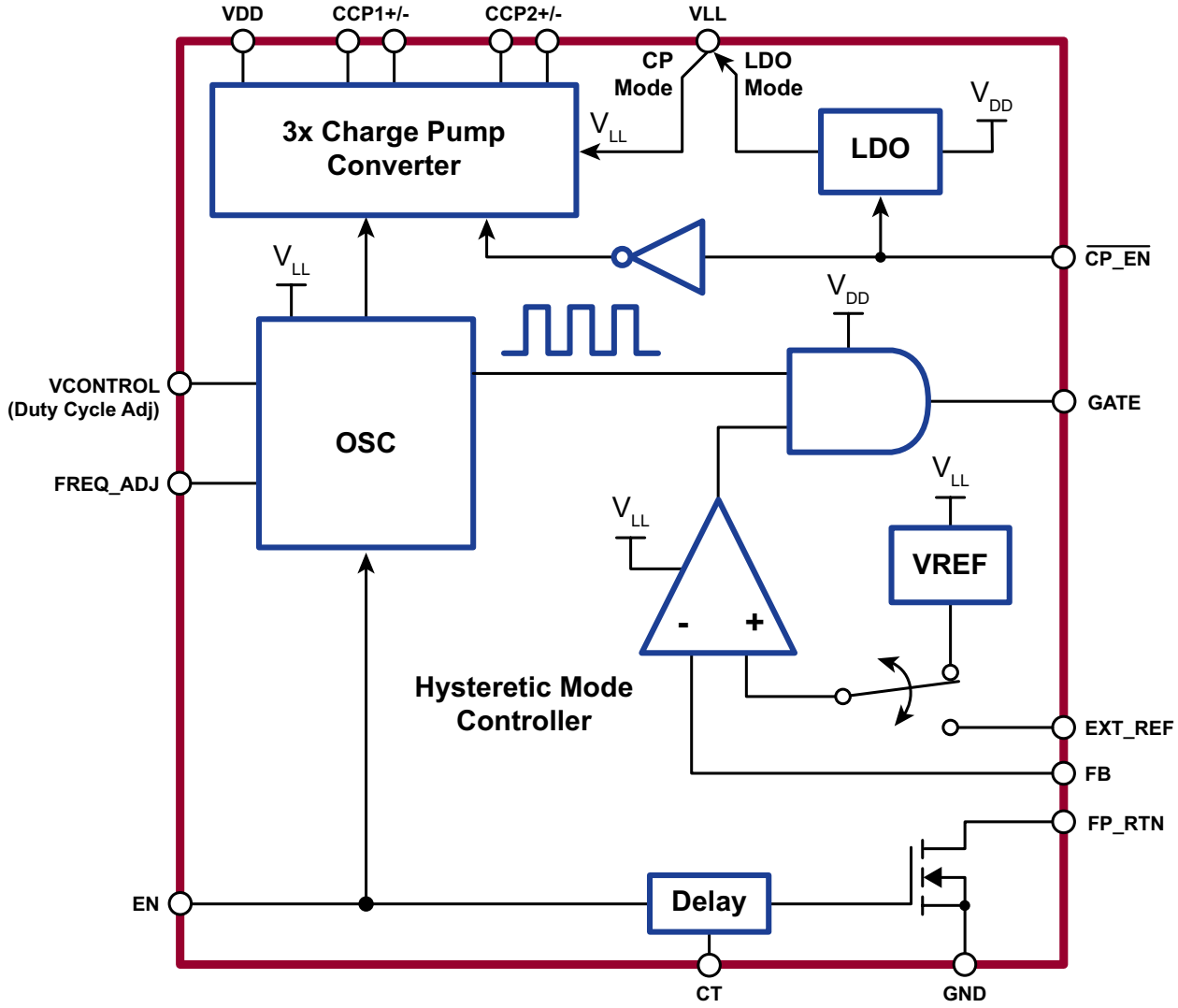
Sym	Description		Min	Typ	Max	Unit	Conditions
Feedback (FB)							
V_{REF}	Internal feedback reference voltage	Accuracy	1.22	1.25	1.28	V	---
		Range	1.20	1.25	1.30		T_j = -25 to 85°C
I_{BIAS}	Input bias current		-	-	1.0	µA	EXT_REF is selected
EXT_REF	External reference voltage	Range	0	-	V_{LL}-1.4	V	---
		Trigger INT reference	0	-	0.12	V	During EN positive triggering
		Trigger EXT reference	0.5	-	V_{LL}-1.4	V	
FB_RTN	ON-resistance, R_{DS}		-	-	500	Ω	I_O = 2.0mA
	Breakdown voltage, BV		-	-	13.5	V	---
GATE Driver Output (GATE)							
t_R	Rise time		-	-	36	ns	C_L = 300pF, V_{DD} = 12V
t_F	Fall time		-	-	12	ns	
R_{UP}	Pull up resistance	V_{DD} = 5.0V	-	-	45	Ω	I_O = 20mA
		V_{DD} = 12V	-	-	30		I_O = 50mA
R_{DOWN}	Pull down resistance	V_{DD} = 5.0V	-	-	15	Ω	I_O = 20mA
		V_{DD} = 12V	-	-	12		I_O = 50mA

AC Electrical Characteristics

(Over recommended operating supply voltages and temperatures unless otherwise noted, T_J = 25°C)

Sym	Description		Min	Typ	Max	Unit	Conditions
f_{GATE}	Oscillator frequency		-	½ f_{OSC}	-	kHz	---
Charge Pump Converter							
V_{DD}	Charge pump output voltage		5.0	$3V_{LL}$-1.8	12.6	V	2.7V ≤ V_{LL} ≤ 4.5V C_{CP1} = 220nF C_{CP2} = 220nF C_{CP3} = 220nF
f_{OSC}	Oscillator frequency	Accuracy	170	195	220	kHz	R_{FREQ} = 270kΩ, V_{LL} = 3.3V
		Range	40	-	400		Over R_{FREQ} range
Δf	Oscillator frequency tolerance		-	15	-	%	50kHz ≤ f_{OSC} ≤ 250kHz
DC	Duty cycle	Accuracy	86	87.5	89	%	R_{FREQ} = 270kΩ
		Range	-	0	-	%	0< V_{CNTL} ≤ 0.18V_{LL}
			-	50	-	%	0.22V_{LL} < V_{CNTL} ≤ 0.38V_{LL}
			-	62.5	-	%	0.42V_{LL} < V_{CNTL} ≤ 0.58V_{LL}
			-	75	-	%	0.62V_{LL} < V_{CNTL} ≤ 0.78V_{LL}
			-	87.5	-	%	0.82V_{LL} < V_{CNTL} ≤ V_{LL}
$V_{CONTROL}$	Duty cycle adjustment		0	-	V_{LL}	V	See table
R_{FREQ}	Frequency adjustment resistor		120k	-	1.2M	Ω	---
R_{CP}	Maximum charge pump output resistance	Pull up	-	-	20	Ω	V_{LL} = 2.7V, I_O = 10mA
		Pull down	-	-	20		
V_{RIPPLE}	Output ripple at V_{DD}		-	-	100	mV	2.7V ≤ V_{LL} ≤ 4.5V f_{OSC} = 200kHz C_{CP1} = 220nF C_{CP2} = 220nF C_{CP3} = 220nF C_{GATE} = 300pF BW = 20MHz
Delay Timer							
T_{DELAY}	Shutdown delay timer		-	240	-	ms	C_T = 1.0µF

Functional Block Diagram



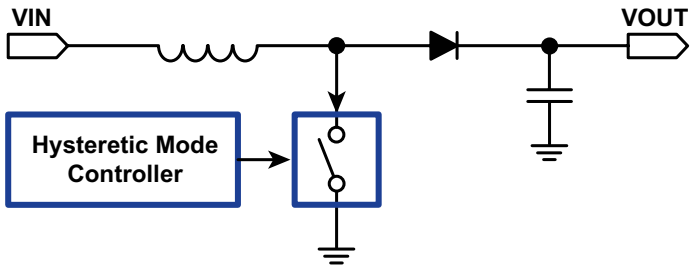
Functional Description

Hysteretic Mode Controller

A hysteretic mode controller consists of an oscillator, a voltage reference, a comparator and a driver. Both the internal oscillator and the duty cycle of the gate driver are running at a fixed rate.

As this device is designed for a step up conversion, a pulse train is used to control the switch of a classical switching boost converter. The pulse train is gated by the output of the comparator, which compares the feedback of the output voltage with the voltage reference.

If the output voltage reaches the target voltage, the comparator will turn off the pulse train. When the output voltage drops below the target voltage, the comparator will pass the pulse train to the switch and start the inductor charging cycle. The advantage of this hysteretic mode controller is its stability and simple operation.



Hysteretic Mode Controller and a Classical Boost Converter

Internal Oscillator

This device has an internal oscillator which generates the reference clock for the hysteretic mode controller. The controller is running at half of the frequency of the internal oscillator. This oscillator is powered by the VLL power supply pin.

The frequency of the oscillator is set by the external resistor R_{FREQ}, and this frequency is inversely proportional to the value of R_{FREQ}. Its characteristic is shown in the f_{OSC} vs R_{FREQ} diagram.

$$f_{OSC} = \frac{1}{4 \cdot R_{FREQ} \cdot C}$$

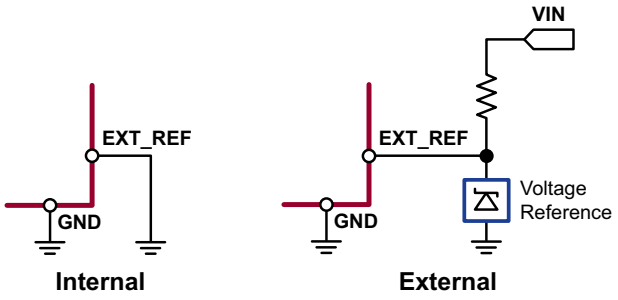
where C = 4.75pF

Voltage Reference (VREF)

The voltage reference is used by the comparator to compare with the feedback voltage and the boost converter output. This device provides the options of using either its internal voltage reference or an external voltage reference.

The internal voltage reference provides a stable 1.25V with a tolerance of ±2.5%. With the use of ±1% tolerance feedback resistors, the output can be achieved with a tolerance of ±4.5%. In order to use the internal voltage reference, the EXT_REF pin must be connected to ground.

If the output voltage of the boost converter is required to have high precision and tight tolerance, the external voltage reference can be used to achieve that purpose. The external reference voltage must be between 0.5V and V_{LL} -1.4V, and connect to the EXT_REF pin. A single low to high transition must be presented at the EN pin to trigger the device to select an external voltage reference. If no enable control signal is available in the application, this signal can be easily mimicked by a simple RC circuit.



Voltage Connection Reference

Gate Driver (GATE)

The MOSFET gate driver of this controller is specially designed to be able to drive the gate of the external MOSFET up to 12V. A high pulse voltage will help to minimize the ON-resistance of the external MOSFET transistor. A lower ON-resistance improves the overall efficiency and heat dissipation.

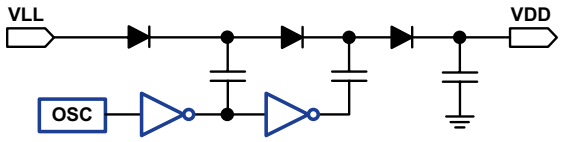
This gate driver is powered by the supply voltage V_{DD} which can be generated by either the internal charge pump converter (CP mode) or the external power supply (LDO mode), depending on the available voltage supply rail of the application.

Charge Pump Converter (CP mode)

A 3x charge pump converter is integrated into this device to provide a 5V to 12V rail for the gate driver. It can be activated by setting $\overline{CP\_EN}$ to ground. A 3.3V supply is more common and easily available for digital logic systems; however, this voltage level is less desirable for driving a high voltage MOSFET to obtain a lower ON-resistance for better efficiency.

In order to reduce the number of supply rails used in the system, an internal two stage charge pump converter is added, which can boost the 3.3V supply voltage to 8.0V. A 8.0V gate driver output will outperform a 3.3V gate driver by far and substantially improves the ON-resistance of the external MOSFET.

The charge pump input can operate with an input voltage from 2.7V to 4.5V. Its input and output are connected to the VLL and VDD pins, respectively.



Three Times (3X) Charge Pump Converter

Linear Regulator (LDO mode)

In some applications, efficiency may be a key factor, and higher voltage rails such as 5V, 6V, 9V or 12V may be available in the system. The internal charge pump converter cannot operate with these voltage levels because of the maximum output voltage limit of the charge pump converter. At the same time, these voltage levels are high enough to provide an adequate supply for the gate driver.

Under this circumstance, an internal linear regulator is used to replace the charge pump converter. This linear regulator input can accept voltage from 5.0V to 12.0V, and generates a 3.3V output to supply to the internal circuit. This linear regulator can be activated by setting $\overline{CP\_EN}$ to VLL.

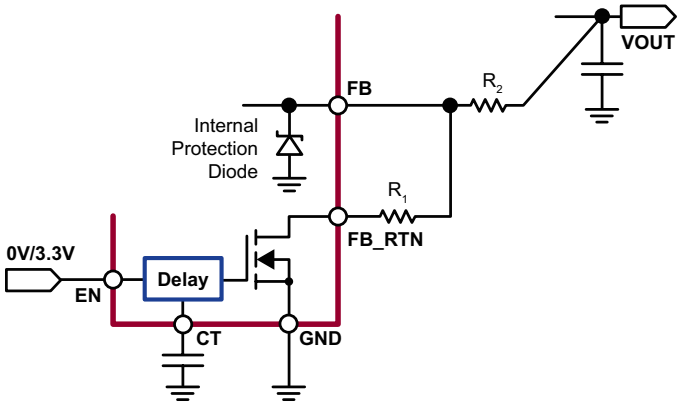
In a scenario when the device is operating in LDO mode and in shutdown state (EN = ”0”), the voltage at VLL is undefined. In order to wake up the controller device, a voltage above 2.7V has to be presented at the enable pin (EN).

FB Ground Return Switch (FB_RTN)

Any DC/DC controller requires a feedback from the output to monitor its operation so that it can regulate its output accordingly. A simple resistor network is used in conjunction with a feedback ground switch as a feedback path. The purpose of this feedback ground switch is to save power consumed by the feedback resistor network when the controller is disabled. This function is quite useful for power saving especially for battery operated applications.

Shutdown Timer and Timing Capacitor (C_T)

A shutdown timer is also integrated into the controller for safety purposes. When the controller shuts down from its normal operation, the converter initial output is still at its high level. If the feedback ground return switch is disabled at the same time, a current path is created from the output via the feedback resistor, and the internal protection clamping diode at the FB pin. Depending upon the value of the FB resistor, this momentarily conducting current can be high enough to damage this clamping diode. In order to avoid this potential problem, a timer is added to the disable function to keep the feedback ground switch to the on position for a short period of time. This on time duration is controlled by an external capacitor C_T. The larger the capacitor value is, the longer this on time is. Its characteristic is shown in the performance section.



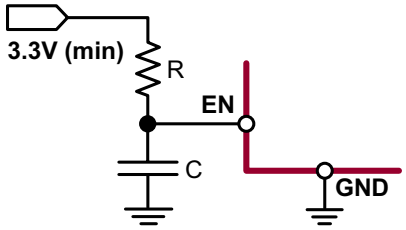
Internal Protection Diode at FB Pin

Hysteretic Controller Enable (EN)

The controller enable pin (EN), serves two main purposes. The most obvious function is to turn the controller on and off, and the other function is to act as a trigger to activate the device to accept external voltage reference.

For any applications required a highly precise voltage reference, an external voltage reference should be used. To activate the device to accept the external voltage reference, a low to high transition has to appear at the EN pin while the voltage at the EXT_REF pin is above 0.5V.

If the system lacks enable function control, a RC circuit can be used to mimic this function to allow the external voltage reference.

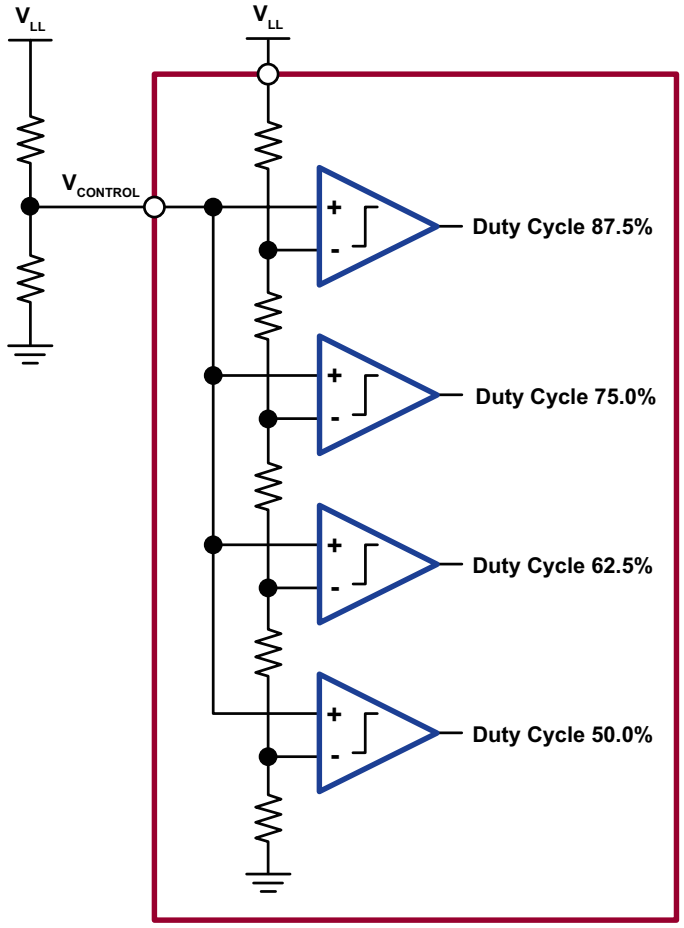


Simple RC Circuit for EN Pin

Duty Cycle Control (VCONTROL)

The input voltage at the VCONTROL pin controls the duty cycle of the internal oscillator output to the GATE driver. The internal comparators are all powered by the V_{LL} supply and their input threshold voltages are all referenced to V_{LL} voltage. A voltage divider formed by the two resistors can be adjusted accordingly to select the desired duty cycle of the pulse signal to the gate driver. Please see the table below.

VCONTROL	Duty Cycle
0 to 0.18V_{LL}	0%
0.22 to 0.38V_{LL}	50%
0.42 to 0.58V_{LL}	62.5%
0.62 to 0.78V_{LL}	75%
0.82 to 1.0V_{LL}	87.5%



Design Procedure

There are several parameters that a user will decide for the DC/DC converter design. The input voltage, output voltage and output power requirement are usually defined at the beginning. The few parameters that the user needs to decide on include: operating frequency, inductor value, duty cycle and the ON-resistance of the MOSFET. There is some degree of flexibility in deciding the values of these parameters. The following provides the user a general approach to this subject.

Step 1

Since this DC/DC controller device is operating in a discontinuous conduction mode, the following equations are used to determine the inductance and the switching frequency.

Given:

D = duty cycle
R = load resistance of the high voltage output
V_i = minimum input voltage
V_O = output voltage

Unknown:

L = inductance
f_{GATE} = driver switching frequency

$$V_O = \frac{V_i}{2} \bullet \left(1 + \sqrt{1 + \frac{4D^2}{K}}\right)$$

where:

$$K = \frac{2 \bullet L \bullet f_{GATE}}{R}$$

The maximum duty cycle can be determined by the following equation:

$$D_{MAX} = 1 - \frac{V_i}{V_o}$$

Then, the user can choose any duty cycle less than D_{MAX}. It is recommended that the largest possible setting be chosen.

To compensate for the limited efficiency, the user can add the efficiency factor into the load resistance R. With the above equation, the product of L and f_{GATE} is determined. The design will be limited by the product of L and f_{GATE}.

Step 2

The standard inductor is usually sold in an incremental inductance value, for example, 10, 22, 33 or 47µH. The user can choose the inductance based on the size of the inductor, the peak current, the maximum operating frequency and the DC resistance. After the value of L is decided, the gate driver switching frequency can be computed. The required R_{FREQ} resistance can be found in the f_{GATE} vs R_{FREQ} table. Next, the peak current of the inductor is checked by the following equation. The saturation current of the inductor must be larger than I_{PEAK}.

$$I_{PEAK} = \frac{V_i \bullet D}{L \bullet f_{GATE}}$$

Step 3

The most important factors to determine the MOSFET are the breakdown voltage, the current capability, the ON-resistance, the minimum V_{GS} threshold voltage and the input capacitance.

The HV9150 gate driver is designed to drive a maximum of 300pF capacitive load. So, the maximum input capacitance of the external MOSFET should be less than 300pF. The minimum breakdown voltage must be larger than the required DC/DC converter output voltage. If the breakdown voltage is too low, the output will never reach the required voltage output. A MOSFET with high ON-resistance will limit the peak current charging the inductor. The user can use a simple RL charging circuit equation to determine its final charging current.

$$I_L = \frac{V_i}{R_{ON}}\left[1 - exp\left(-\frac{D}{f_{GATE}} \bullet \frac{R_{ON}}{L}\right)\right]$$

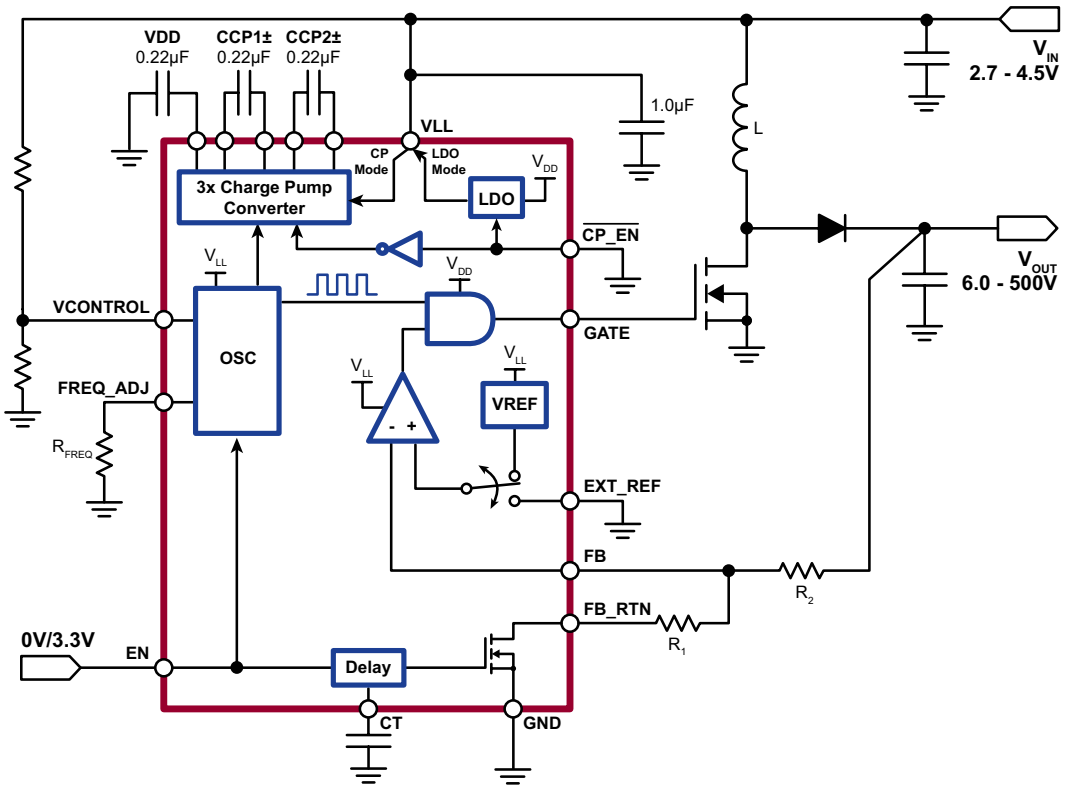
It is recommended that the calculated value of I_L is within 95% of the I_{PEAK} calculated in step 2. An ON-resistance of less than 1Ω is usually a good starting point.

If the final circuit is short on the output current capability, there are a few ways to boost the output. The user can do any or all of the following to improve the output:

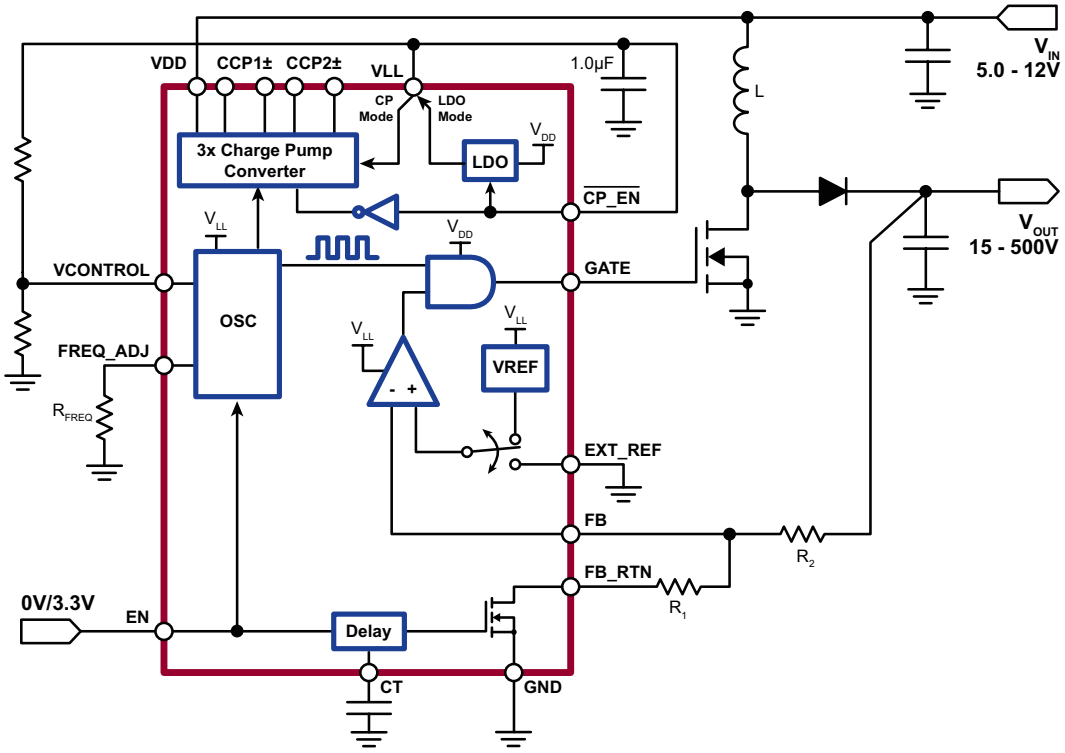
(1) increase the duty cycle
(2) decrease the f_{GATE}
(3) use a MOSFET with lower ON-resistance.

Typical Application Circuits

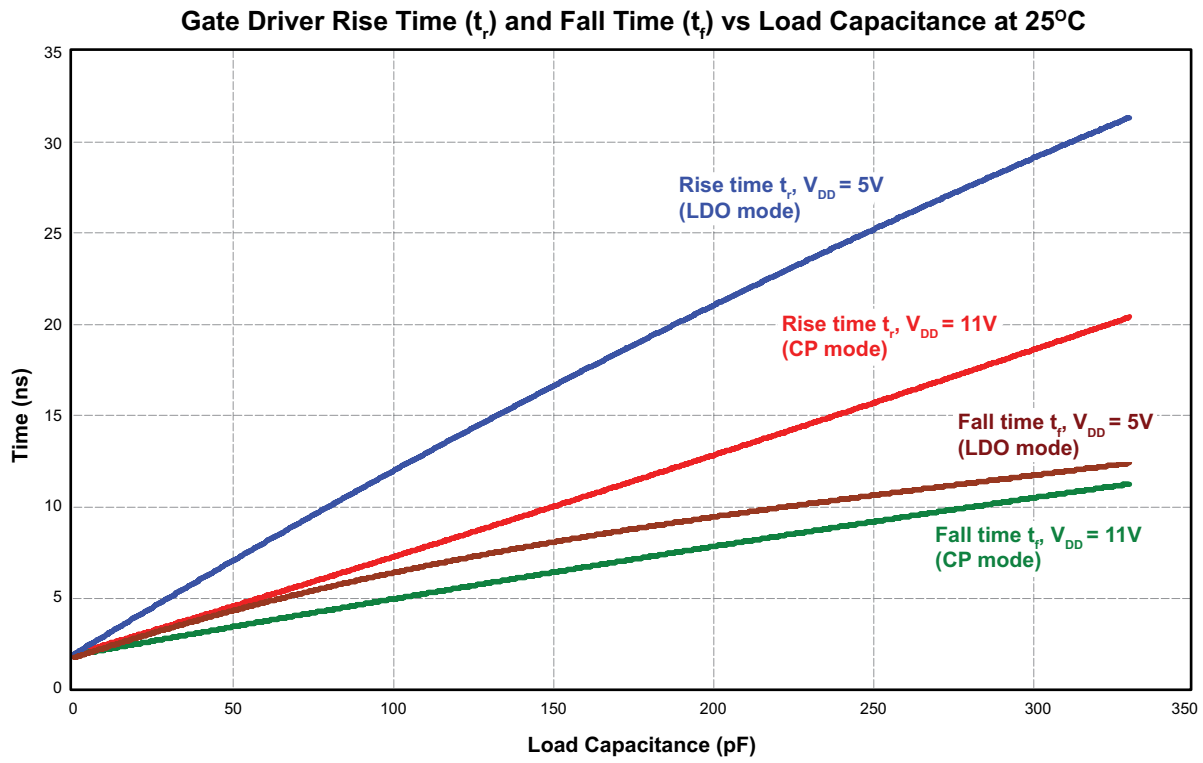
Charge Pump (CP) Mode

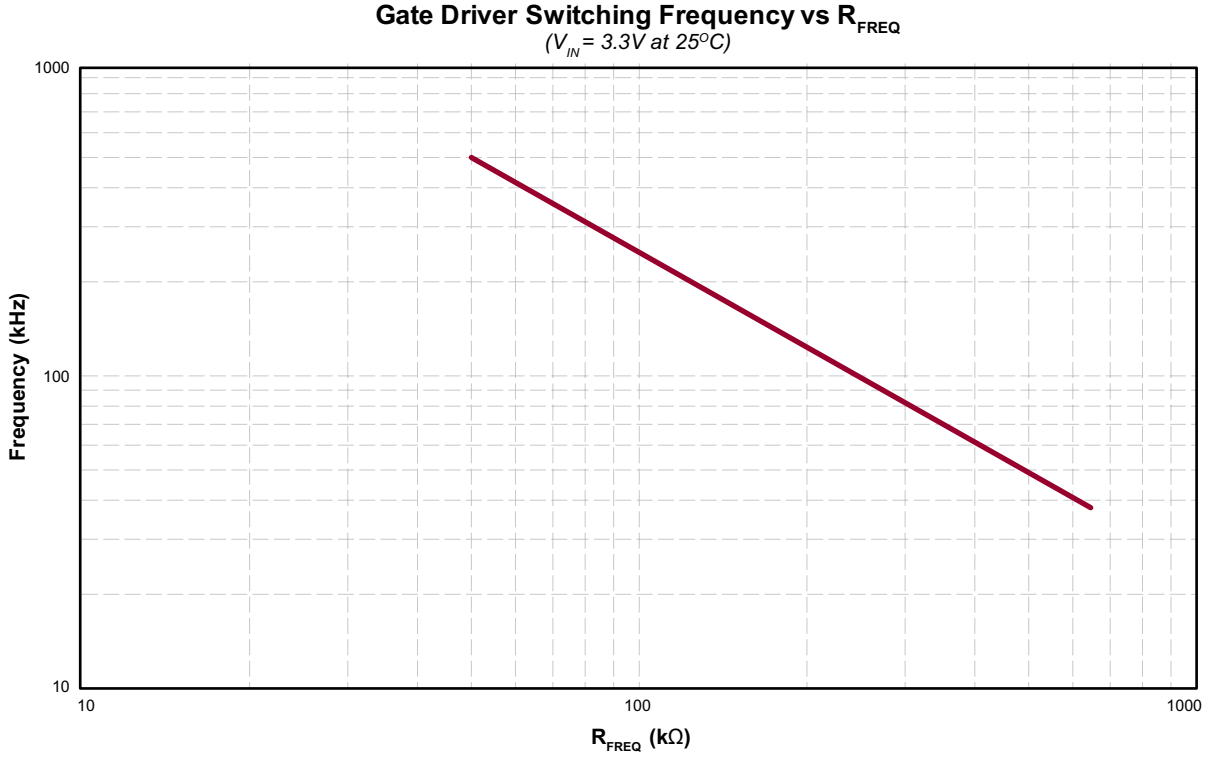


Linear Regulator (LDO) Mode

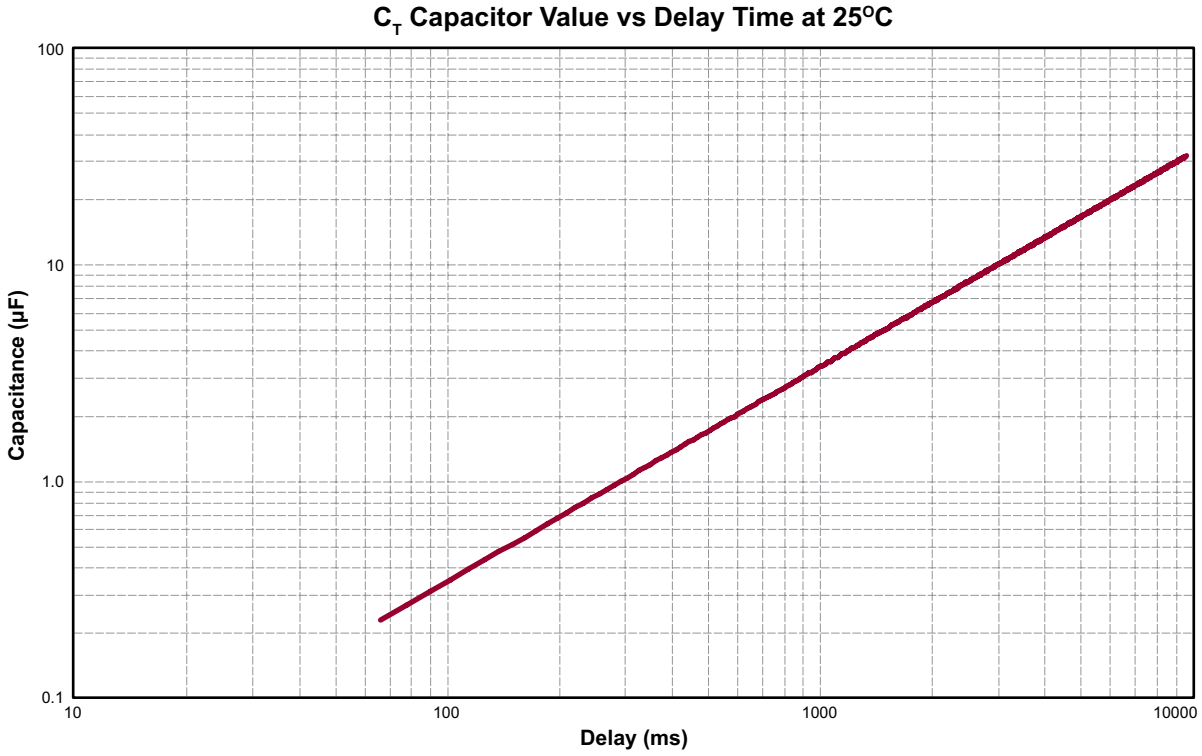


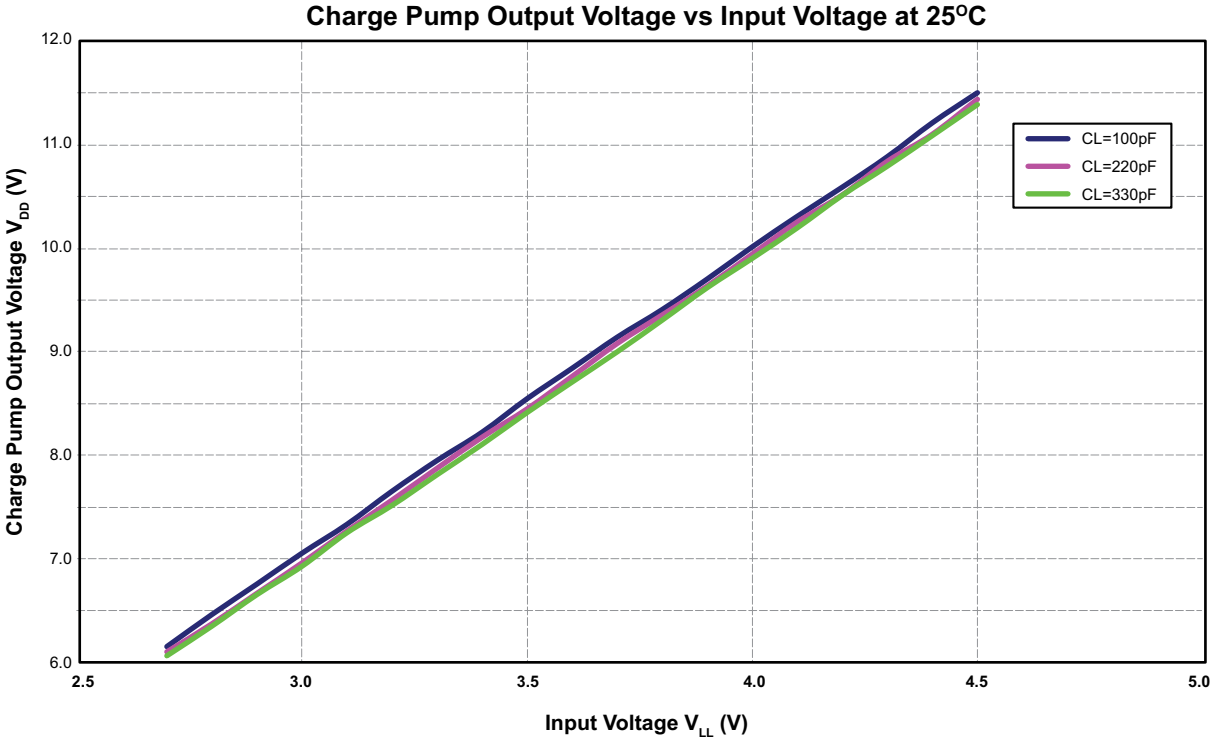
Typical Performance Characteristics





Typical Performance Characteristics *(cont.)*

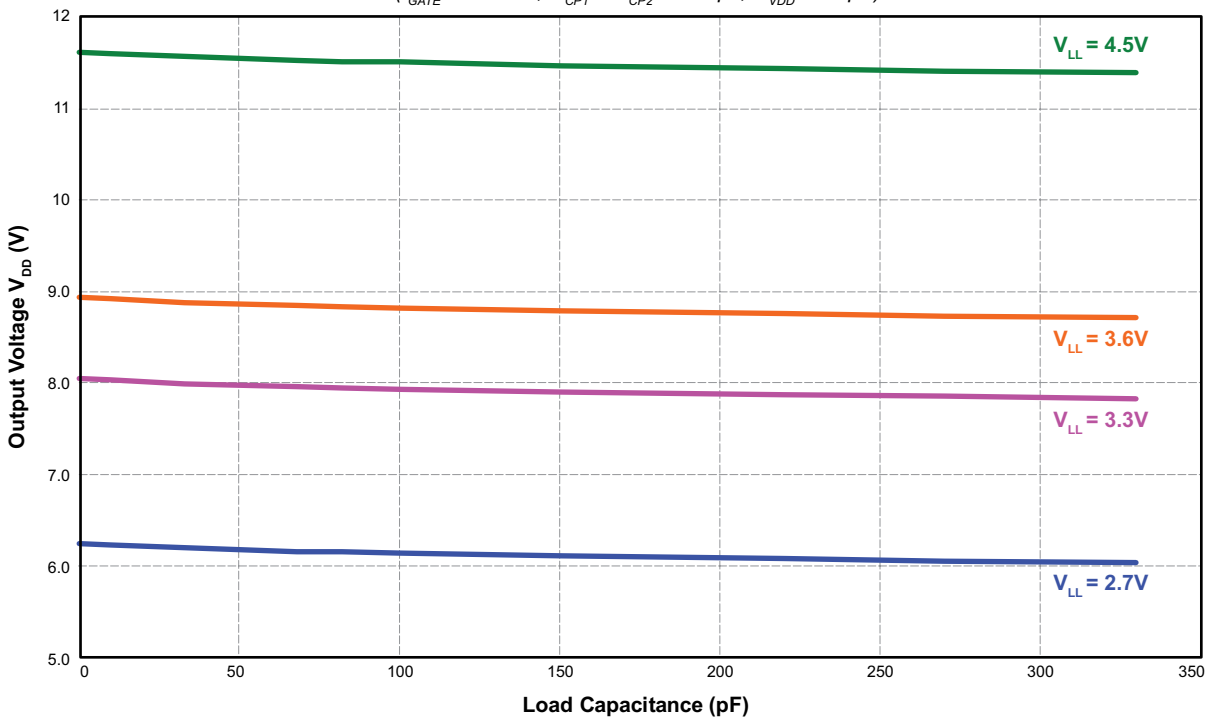




Typical Performance Characteristics *(cont.)*

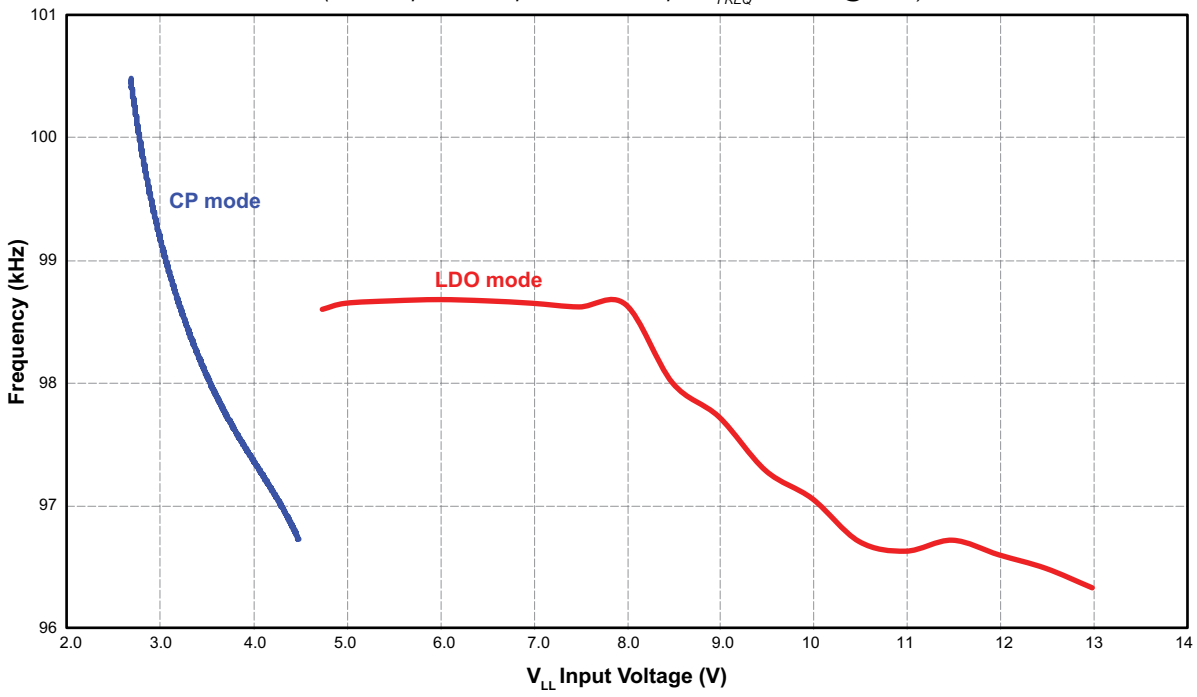
Charge Pump Output Voltage vs Load Capacitance at 25°C

(f_{GATE} = 100kHz, C_{CP1} = C_{CP2} = 0.22µF, C_{VDD} = 1.0µF)

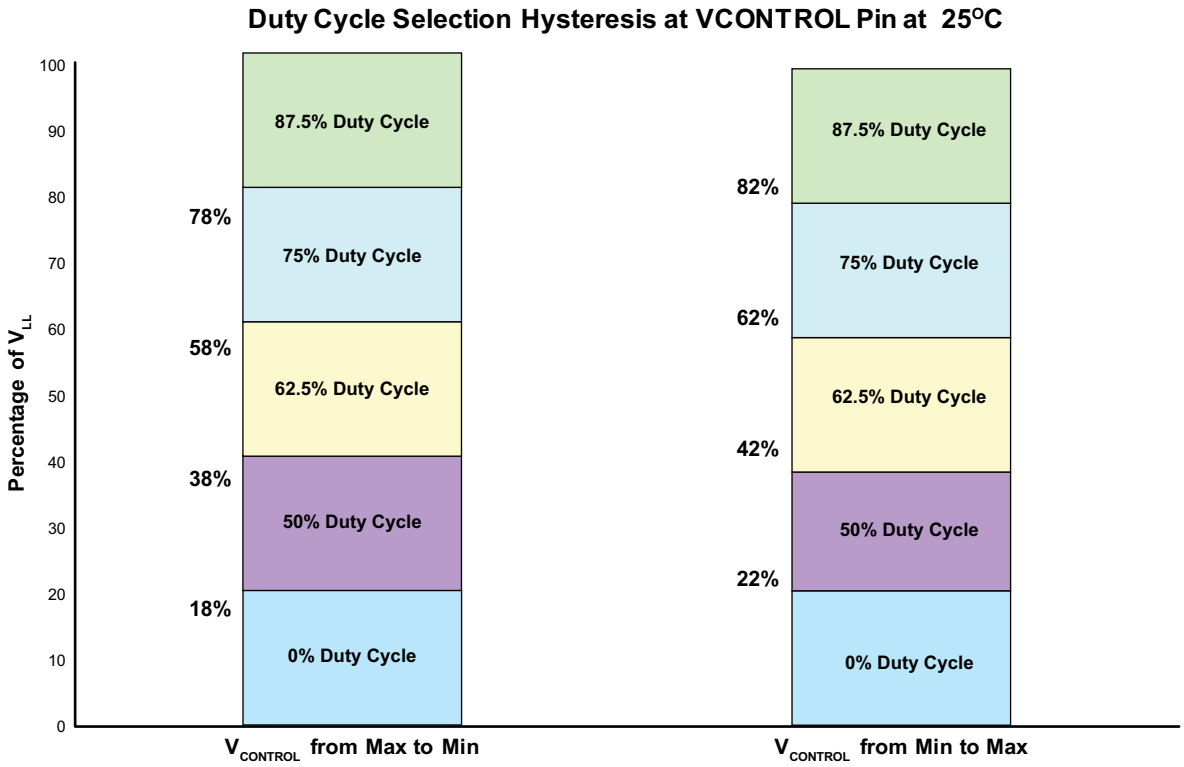


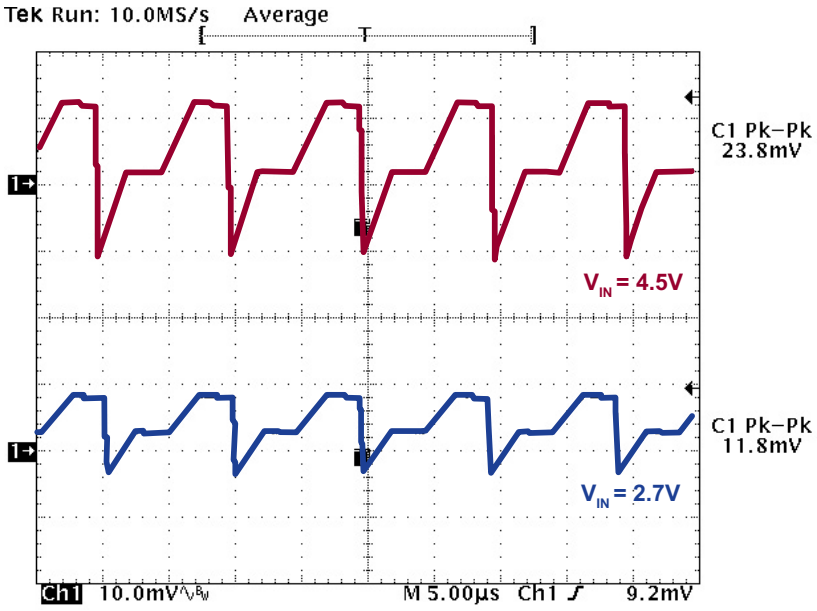
Gate Driver Switching Frequency vs V_{LL} Input Voltage

(Gate output load capacitance = 330pF, R_{FREQ} = 255kΩ @ 25°C)



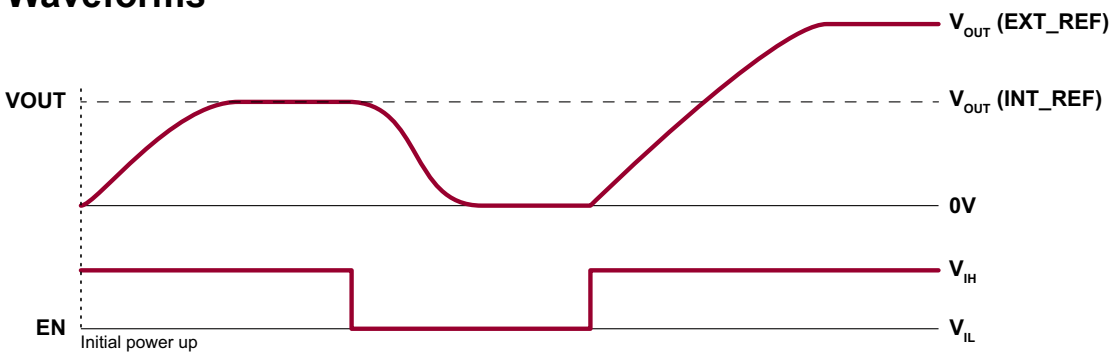
Typical Performance Characteristics *(cont.)*



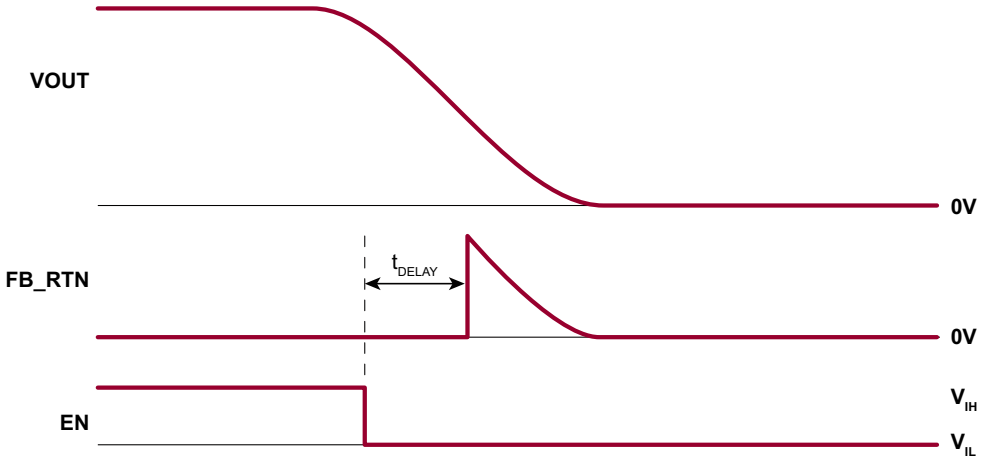


VCP Noise

Switching Waveforms



Enabling to use the External Voltage Reference



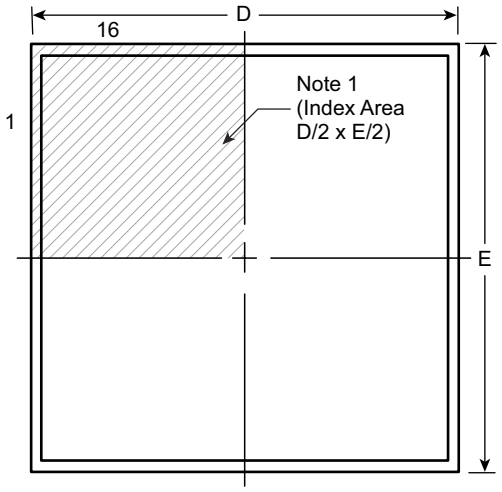
Delay Time at FB_RTN

Pin Description

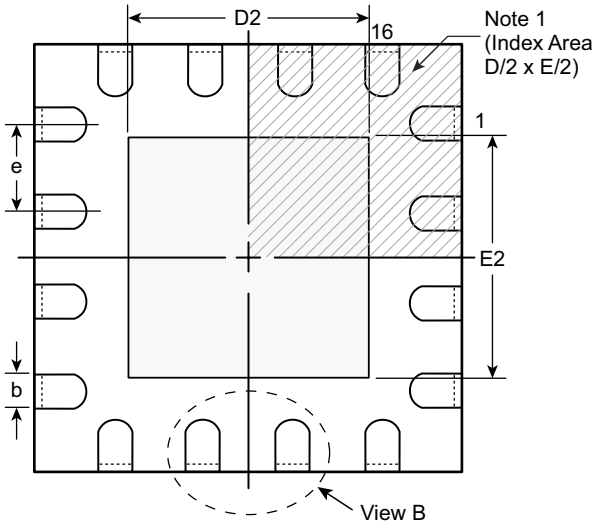
Pin #	Function	Description
1	VLL	Input supply voltage
2	GND	Ground connection
3	EN	Enable
4	$\overline{\text{CP\_EN}}$	Charge pump/LDO enable input
5	VCONTROL	Duty cycle adjustment voltage control input
6	FREQ_ADJ	Frequency adjustment
7	EXT_REF	External reference voltage input
8	CT	Timing capacitor
9	FB	Feedback input voltage
10	FB_RTN	Feedback return
11	GATE	Gate control output
12	VDD	Charge pump output voltage
13	CCP2+	Charge pump storage capacitor #2 plus terminal
14	CCP2-	Charge pump storage capacitor #2 minus terminal
15	CCP1+	Charge pump storage capacitor #1 plus terminal
16	CCP1-	Charge pump storage capacitor #1 minus terminal
Center Pad		Substrate connection (at ground potential)

16-Lead QFN Package Outline (K6)

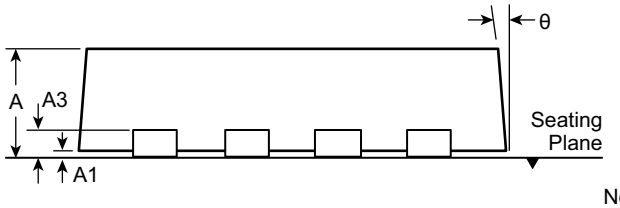
3.00x3.00mm body, 1.00mm height (max), 0.50mm pitch



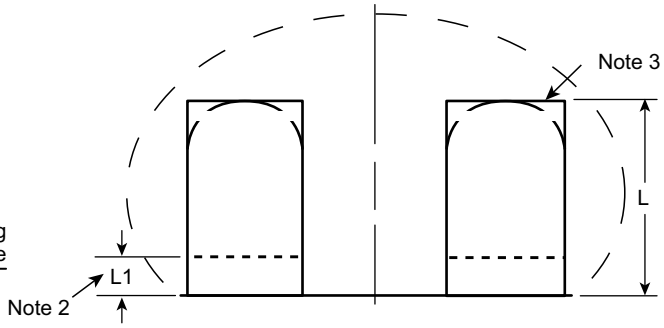
Top View



Bottom View



Side View



View B

Notes:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.*
3. *The inner tip of the lead may be either rounded or square.*

Symbol		A	A1	A3	b	D	D2	E	E2	e	L	L1	θ
Dimension (mm)	MIN	0.80	0.00	0.20 REF	0.18	2.85*	1.50	2.85*	1.50	0.50 BSC	0.20†	0.00	0°
	NOM	0.90	0.02		0.25	3.00	1.65	3.00	1.65		0.30†	-	-
	MAX	1.00	0.05		0.30	3.15*	1.80	3.15*	1.80		0.45	0.15	14°

JEDEC Registration MO-220, Variation VEED-4, Issue K, June 2006.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-16QFNK63X3P050, Version A092909.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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